**IN THE CLAIMS**:

1. (Currently Amended) A method, comprising:

forming a first layer of epitaxial silicon having a thickness of approximately 15-30 microns above a surface of a semiconducting substrate;

forming a second layer of epitaxial silicon having a thickness of approximately 0.5-2.0 microns ~~above~~ on said first layer of epitaxial silicon;

forming a third layer of epitaxial silicon having a thickness of approximately 20-25 microns ~~above~~ on said second layer of epitaxial silicon, wherein said semiconducting substrate is doped with a dopant material of a first type and said second and third layers of epitaxial silicon are doped with a dopant material that is of a type opposite to that of said first type of dopant material, and wherein said first, second and third layers of epitaxial silicon are formed by performing an *in situ* epitaxial growth process in a single epitaxial reactor;

forming a trench isolation region that extends through at least said third layer of epitaxial silicon; and

forming a portion of a semiconductor device above said third layer of epitaxial silicon within an area defined by said isolation region.

2. (Canceled)

3. (Original) The method of claim 1, wherein said semiconducting substrate is doped with a P-type dopant material and said second and third layers of epitaxial silicon are doped with an N-type dopant material.

4. (Original) The method of claim 1, wherein said semiconducting substrate is doped with an N-type dopant material and said second and third layers of epitaxial silicon are doped with a P-type dopant material.

5. (Original) The method of claim 1, wherein said first layer of epitaxial silicon is an undoped layer of epitaxial silicon.

6. (Original) The method of claim 1, wherein said first layer of epitaxial silicon is doped with either a P-type or an N-type dopant material.

7. (Original) The method of claim 1, wherein said second and third layers of epitaxial silicon are doped layers of epitaxial silicon and wherein said second layer of epitaxial silicon has a greater concentration level of dopant material than said third layer of epitaxial silicon.

8. (Canceled)

9. (Original) The method of claim 1, wherein said substrate has a dopant concentration of approximately $1e^{17}$-$5e^{17}$ ions/$cm^3$ of a P-type dopant material.

10. (Original) The method of claim 9, wherein said first layer of epitaxial silicon has a dopant concentration less than approximately $1e^{15}$ ions/$cm^3$ of an N-type dopant material.

11. (Original) The method of claim 9, wherein said second layer of epitaxial silicon has a dopant concentration greater than approximately $5e^{17}$ ions/$cm^3$ of an N-type dopant material.

12. (Original) The method of claim 9, wherein said third layer of epitaxial silicon has a dopant concentration of approximately $5e^{14}$-$1e^{15}$ ions/$cm^3$ of an N-type dopant material.

13. (Original) The method of claim 1, wherein said substrate has a dopant concentration of approximately $1e^{17}$-$5e^{17}$ ions/$cm^3$ of an N-type dopant material.

14. (Original) The method of claim 13, wherein said first layer of epitaxial silicon has a dopant concentration less than approximately $1e^{15}$ ions/$cm^3$ of a P-type dopant material.

15. (Original) The method of claim 13, wherein said second layer of epitaxial silicon has a dopant concentration greater than approximately $5e^{17}$ ions/$cm^3$ of a P-type dopant material.

16. (Original) The method of claim 13, wherein said third layer of epitaxial silicon has a dopant concentration of approximately $5e^{14}$-$1e^{15}$ ions/$cm^3$ of a P-type dopant material.

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Original) The method of claim 1, wherein forming a trench isolation region comprises:

performing at least one etching process to form a trench that extends through at least said third layer of epitaxial silicon; and

forming at least one insulating material in said trench.

21. (Original) The method of claim 1, wherein said semiconductor device comprises at least one of a bipolar transistor, a resistor, a diode, a logic device and a memory device.

22. (Currently Amended) A method, comprising:

forming a first layer of epitaxial silicon <u>having a thickness of approximately 15-30 microns</u> above a surface of a semiconducting substrate, said semiconducting substrate being doped with a first type of dopant material;

forming a second layer of epitaxial silicon <u>having a thickness of approximately 0.5-2.0 microns</u> ~~above~~ <u>on</u> said first layer of epitaxial silicon, said second layer of epitaxial silicon being doped with a dopant material that is of a type opposite to that of said first type of dopant material;

forming a third layer of epitaxial silicon having a thickness of approximately 20-25 microns ~~above~~ on said second layer of epitaxial silicon, said third layer of epitaxial silicon being doped with a dopant material that is of a type opposite to that of said first type of dopant material, wherein said second layer of epitaxial silicon has a greater concentration level of dopant material than said third layer of epitaxial silicon, wherein said first, second and third layers of epitaxial silicon are formed by performing an *in situ* epitaxial growth process in a single epitaxial reactor;

forming a trench isolation region that extends through at least said third layer of epitaxial silicon; and

forming a semiconductor device above said third layer of epitaxial silicon within an area defined by said isolation region.

23. (Original) The method of claim 22, wherein said semiconducting substrate is doped with a P-type dopant material and said second and third layers of epitaxial silicon are doped with an N-type dopant material.

24. (Original) The method of claim 22, wherein said semiconducting substrate is doped with an N-type dopant material and said second and third layers of epitaxial silicon are doped with a P-type dopant material.

25. (Original) The method of claim 22, wherein said first layer of epitaxial silicon is an undoped layer of epitaxial silicon.

26. (Original) The method of claim 22, wherein said first layer of epitaxial silicon is doped with either a P-type or an N-type dopant material.

27. (Canceled)

28. (Original) The method of claim 22, wherein said substrate has a dopant concentration of approximately $1e^{17}$-$5e^{17}$ ions/$cm^3$ of a P-type dopant material.

29. (Original) The method of claim 28, wherein said first layer of epitaxial silicon has a dopant concentration less than approximately $1e^{15}$ ions/$cm^3$ of an N-type dopant material.

30. (Original) The method of claim 28, wherein said second layer of epitaxial silicon has a dopant concentration greater than approximately $5e^{17}$ ions/$cm^3$ of an N-type dopant material.

31. (Original) The method of claim 28, wherein said third layer of epitaxial silicon has a dopant concentration of approximately $5e^{14}$-$1e^{15}$ ions/$cm^3$ of an N-type dopant material.

32. (Original) The method of claim 22, wherein said substrate has a dopant concentration of approximately $1e^{17}$-$5e^{17}$ ions/$cm^3$ of an N-type dopant material.

33. (Original) The method of claim 32, wherein said first layer of epitaxial silicon has a dopant concentration less than approximately $1e^{15}$ ions/$cm^3$ of a P-type dopant material.

34. (Original) The method of claim 32, wherein said second layer of epitaxial silicon has a dopant concentration greater than approximately $5e^{17}$ ions/$cm^3$ of a P-type dopant material.

35. (Original) The method of claim 32, wherein said third layer of epitaxial silicon has a dopant concentration of approximately $5e^{14}$-$1e^{15}$ ions/$cm^3$ of a P-type dopant material.

36. (Canceled)

37. (Canceled)

38. (Canceled)

39. (Original) The method of claim 22, wherein forming a trench isolation region comprises:

performing at least one etching process to form a trench that extends through at least said third layer of epitaxial silicon; and

forming at least one insulating material in said trench.

40. (Original) The method of claim 22, wherein said semiconductor device comprises at least one of a bipolar transistor, a resistor, a diode, a logic device and a memory device.

41. (Currently Amended) A method, comprising:

performing an *in situ* epitaxial growth process in a single epitaxial reactor to form:

a first layer of epitaxial silicon having a thickness of approximately 15-30 microns above a surface of a semiconducting substrate, said semiconducting substrate being doped with a first type of dopant material,

a second layer of epitaxial silicon having a thickness of approximately 0.5-2.0 microns ~~above~~ on said first layer of epitaxial silicon, said second layer of epitaxial silicon being doped with a dopant material that is of a type opposite to that of said first type of dopant material, and

a third layer of epitaxial silicon having a thickness of approximately 20-25 microns ~~above~~ on said second layer of epitaxial silicon, said third layer of epitaxial silicon being doped with a dopant material that is of a type opposite to that of said first type of dopant material, wherein said second layer of epitaxial silicon has a greater concentration level of dopant material than said third layer of epitaxial silicon;

forming a trench isolation region that extends through at least said second and third layers of epitaxial silicon by performing at least one etching process to form a trench that extends through at least said second and third layers of epitaxial silicon and forming at least one insulating material in said trench; and

forming a semiconductor device above said third layer of epitaxial silicon within an area defined by said isolation region.

42. (Original) The method of claim 41, wherein said semiconducting substrate is doped with a P-type dopant material and said second and third layers of epitaxial silicon are doped with an N-type dopant material.

43. (Original) The method of claim 41, wherein said semiconducting substrate is doped with an N-type dopant material and said second and third layers of epitaxial silicon are doped with a P-type dopant material.

44. (Original) The method of claim 41, wherein said first layer of epitaxial silicon is an undoped layer of epitaxial silicon.

45. (Original) The method of claim 41, wherein said first layer of epitaxial silicon is doped with either a P-type or an N-type dopant material.

46. (Canceled)

47. (Original) The method of claim 41, wherein said semiconductor device comprises at least one of a bipolar transistor, a resistor, a diode, a logic device and a memory device.

48. (Original) The method of claim 41, wherein said substrate has a dopant concentration of approximately $1e^{17}$-$5e^{17}$ ions/$cm^3$ of a P-type dopant material.

49. (Original) The method of claim 48, wherein said first layer of epitaxial silicon has a dopant concentration less than approximately $1e^{15}$ ions/$cm^3$ of an N-type dopant material.

50. (Original) The method of claim 48, wherein said second layer of epitaxial silicon has a dopant concentration greater than approximately $5e^{17}$ ions/$cm^3$ of an N-type dopant material.

51. (Original) The method of claim 48, wherein said third layer of epitaxial silicon has a dopant concentration of approximately $5e^{14}$-$1e^{15}$ ions/$cm^3$ of an N-type dopant material.

52. (Original) The method of claim 41, wherein said substrate has a dopant concentration of approximately $1e^{17}$-$5e^{17}$ ions/$cm^3$ of an N-type dopant material.

53. (Original) The method of claim 52, wherein said first layer of epitaxial silicon has a dopant concentration less than approximately $1e^{15}$ ions/$cm^3$ of a P-type dopant material.

54. (Original) The method of claim 52, wherein said second layer of epitaxial silicon has a dopant concentration greater than approximately $5e^{17}$ ions/$cm^3$ of a P-type dopant material.

55. (Original) The method of claim 52, wherein said third layer of epitaxial silicon has a dopant concentration of approximately $5e^{14}$-$1e^{15}$ ions/$cm^3$ of a P-type dopant material.

56.-93. (Canceled)